WHAT IS CLAIMED IS:

1. A method for forming a crystalline silicon nitride layer, comprising the steps of:

providing a crystalline silicon substrate with an exposed surface;

precleaning the exposed surface by employing a hydrogen prebake; and

exposing the exposed surface to nitrogen to form a crystalline silicon nitride layer.

2. The method as recited in claim 1, wherein the step of precleaning includes the step of employing a hydrogen fluoride wet clean process to remove native oxide from the exposed surface.

3. The method as recited in claim 2, wherein the step of precleaning the exposed surface by employing a hydrogen prebake is delayed from the step of employing a hydrogen fluoride wet clean process to remove native oxide from the exposed surface by an interval of between about 30 seconds and about 3600 seconds.

4. The method as recited in claim 1, wherein the step of precleaning includes the step of prebaking the exposed surface in the presence of hydrogen gas at a temperature between about 400 °C and about 1300 °C.

5. The method as recited in claim 1, wherein the step of precleaning includes the step of prebaking the exposed surface in the presence of hydrogen gas at a pressure between about 10^{-9} Torr and about 600 Torr.

6. The method as recited in claim 1, wherein the nitrogen includes at least one of nitrogen gas, ammonia, atomic nitrogen plasma, an organic nitrogen precursor and an inorganic nitrogen precursor.

7. The method as recited in claim 1, wherein the step of exposing the exposed surface to nitrogen to form a crystalline silicon nitride layer includes the step of introducing ammonia at a temperature of between about 400 °C and about 1300 °C.

8. The method as recited in claim 1, wherein the step of exposing the exposed surface to nitrogen to form a crystalline silicon nitride layer includes the step of maintaining ammonia at a pressure of between about 10^{-6} Torr and about one atmosphere.

9. A semiconductor device fabricated in accordance with the method as recited in claim 1.

10. A method for forming a node dielectric layer in

deep trenches, comprising the steps of:

providing a crystalline silicon substrate with trenches formed therein, the trenches including exposed silicon surfaces;

precleaning the exposed surfaces by employing a hydrogen prebake;

exposing the exposed surfaces to ammonia to form a crystalline silicon nitride layer;

depositing an amorphous silicon nitride layer over the crystalline silicon nitride layer; and

oxidizing the amorphous silicon nitride layer to form a node dielectric layer.

11. The method as recited in claim 10, further comprising the step of employing a hydrogen fluoride clean process to remove native oxide from the exposed surfaces.

12. The method as recited in claim 11, wherein the step of precleaning the exposed surfaces by employing a hydrogen prebake is delayed from the step of employing a hydrogen fluoride clean process to remove native oxide from the exposed surfaces by an interval of between about 30 seconds and about 3600 seconds.

13. The method as recited in claim 10, wherein the step of precleaning includes the step of prebaking the

exposed surfaces in the presence of hydrogen gas at a temperature between about 400 °C and about 1300 °C.

14. The method as recited in claim 10, wherein the step of precleaning includes the step of prebaking the exposed surfaces in the presence of hydrogen gas at a pressure between about 10^{-9} Torr and about 600 Torr.

15. The method as recited in claim 10, wherein the step of exposing the exposed surfaces to ammonia to form a crystalline silicon nitride layer includes the step of introducing the ammonia at a temperature of between 400 °C and about 1300 °C.

16. The method as recited in claim 10, wherein the step of exposing the exposed surfaces to ammonia to form a crystalline silicon nitride layer includes the step of maintaining the ammonia at a pressure of between about 10^{-6} Torr and about one atmosphere.

17. A semiconductor device fabricated in accordance with the method as recited in claim 10.

18. A trench capacitor comprising:

a crystalline silicon substrate including deep trenches having surfaces in the substrate substantially

free of native oxide; and

a dielectric stack, including a crystalline silicon nitride layer, formed on the surfaces of the trenches, the dielectric stack for forming a node dielectric between electrodes of the trench capacitor.

19. The trench capacitor as recited in claim 18, wherein the crystalline silicon nitride layer includes a thickness of between about 3 Å and about 40 Å.

20. The trench capacitor as recited in claim 18, wherein the dielectric stack includes an oxidized amorphous nitride layer.